VERTICAL BIPOLAR TRANSISTOR FORMED USING CMOS PROCESSES

ABSTRACT OF THE DISCLOSURE

A vertical bipolar transistor is described which utilizes ion implantation steps which are used to form an nMOS field effect device and a pMOS field effect device. The implantation steps form an n-well, a channel stop p-well region and emitter region which are vertically oriented within a semiconductor substrate. The resulting bipolar device is junction isolated from other circuits formed on the substrate by a p-well region.